TITLE 800G OSFP-RHS 2XDR4 (DR8) 500m Transceivers	DOC No. RFD-20260630100-002	
	REVISION：01	AUTHORIZED BY：Andy Yang
	DATE：2026.06.30	CLASSIFICATION ：Optical Transceivers

1. Product Features

- Hot-pluggable 800G OSFP DR8 form factor
- Silicon photonics MZM solution
- 8x53.125GBd PAM4 electrical and optical interface
- Maximum link length of 500m G.652 SMF fiber
- Operating case temperature 0°C to +70 °C
- Power dissipation < 16W
- MPO receptacles
- Compliant with RoHS 2.0

2. Product Applications

- Data center and cloud networks
- Ethernet and InfiniBand NDR
- 8x100G Ethernet
- 4x200G Ethernet
- 2x400G Ethernet

3. Product Description

The Trilight OSFP transceiver module is designed to support 800G Ethernet link transmission over 500-meter single-mode fiber. The module integrates eight parallel optical channels, each with a center wavelength of 1310nm and an operating rate of 106.25Gbps, using PAM4 modulation format. It can convert eight-channel parallel PAM4 optical signals into corresponding PAM4 electrical outputs, and also supports converting eight-channel PAM4 electrical input signals into parallel optical signals. The module's electrical interface strictly follows the 800GAUI-8 specification defined by the IEEE 802.3ck standard and fully complies with the OSFP MSA standard requirements.

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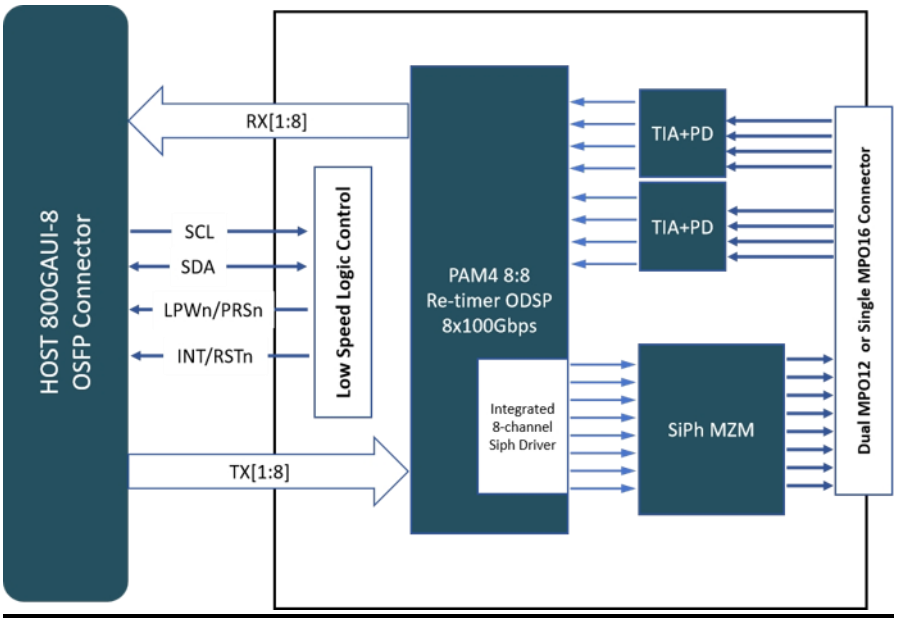

Figure 1: Transceiver Block Diagram

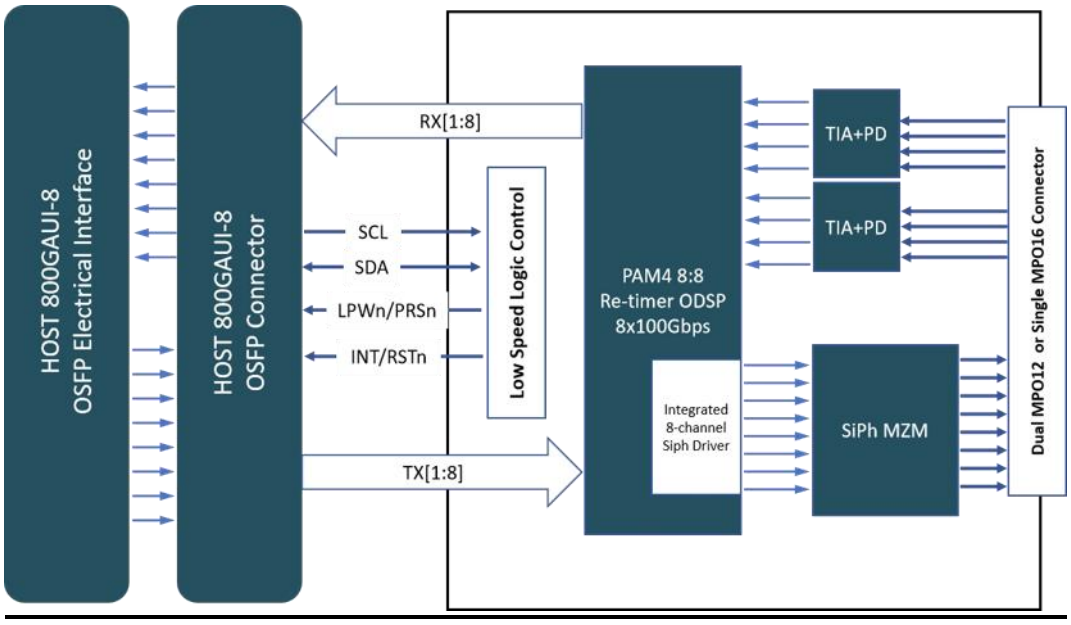

Figure 2: Application Reference Diagram

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Transmitter

As shown in Figure 1, the transmitter path of this transceiver begins with an 8x100Gbps 800GAUI-8 electrical input interface. The input signal first goes through an PAM4 ODSP and is then converted into an 8-channel 100Gbps PAM4 parallel optical signal. This path also integrates a driver, bias circuits for controlling the eight MZ modulators, and single-mode laser light source.

Receiver

As shown in Figure 1, the receiver path of this transceiver converts the 8-channel input optical signal into 8-channel electrical signal output. The receiver includes two 4-channel PIN PD and transimpedance amplifier (TIA), PAM4 ODSP, and an electrical output interface compliant with the 8x100G 800GAUI-8 standard.

High Speed Electrical Signal Interface

The interface between OSFP module and ASIC/SerDes is shown in Figure 2. The high speed signal lines are internally AC-coupled and the electrical inputs are internally terminated to 100 Ohms differential. All transmitter and receiver electrical channels are compliant to module 800GAUI-8 specifications per IEEE 802.3ck.

Control Signal Interface

The control signal interface is compliant with OSFP MSA. The following pin is provided to control module or display the module status: LPWn/PRSn, INT/RSTn. In addition, there is an industry standard two wire serial interface scaled for 3.3V LVTTL. The definition of control signal interface and the registers of the serial interface memory are defined in the Control Interface & Memory Map section.

Handling and Cleaning

This module is an electrostatic discharge sensitive device and should be handled according to relevant protective regulations. It is strictly prohibited to operate it under conditions exceeding the 'absolute maximum rated value.' The module's optical interface is a female connector. When no fiber jumper is inserted, this interface is exposed and must be

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properly protected. To this end, each module comes with port protection plugs. Before inserting the fiber, it is recommended to clean the fiber connector end face to prevent dirt from contaminating the module's optical port. If the port is already contaminated, it should be treated using standard MPO port cleaning tools and methods.

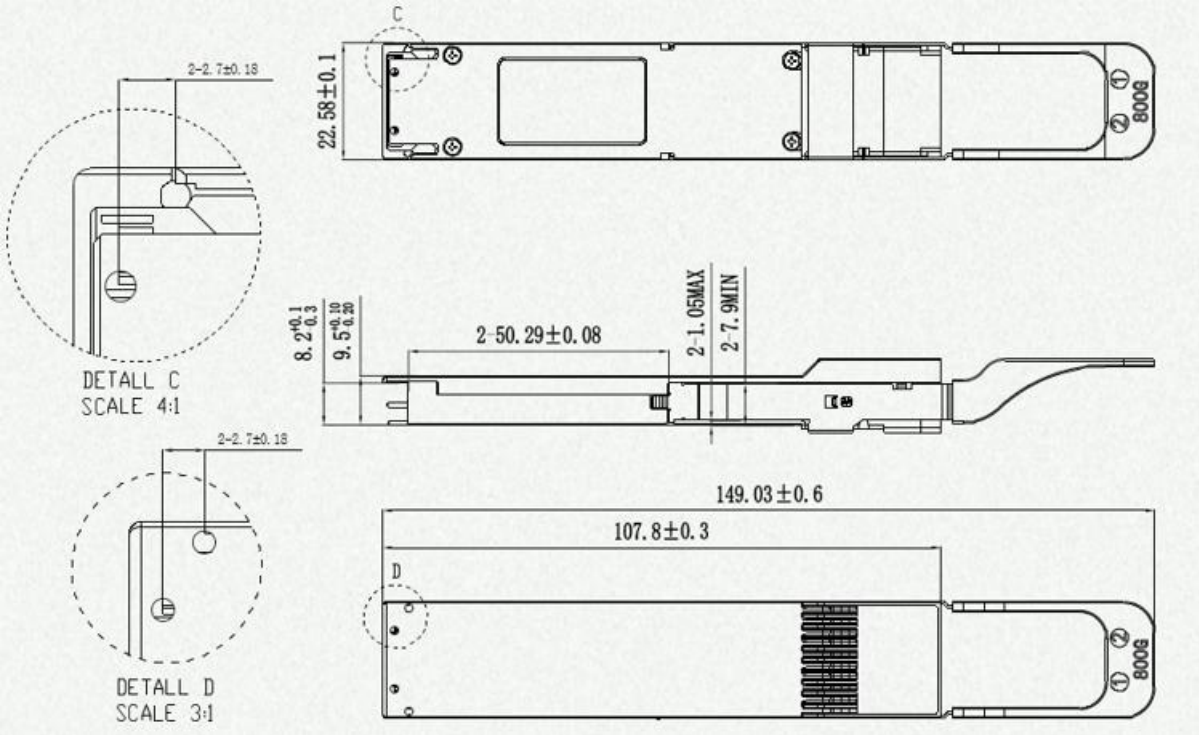
3.1 Product Name And Series Number(S)

800G OSFP 2xDR4 (DR8) 500m Transceivers

JPC P/N	Laser	Distance	Heat Sink	Fiber Type	Connector	Temp.
P69**XKKCBS5-1	1311nm	500m	RHS	SMF	MPO-12/APC	C

Note-1： ** **Indicates the customer code.**

3.2 Dimensions,Materials,Platings And Marking



Unit is millimeter. All dimensions are ±0.1mm unless otherwise specified

The following picture shows the location of the hottest spot for measuring module case temperature. In addition, the digital diagnostic monitors (DDM) temperature is also calibrated to this spot.

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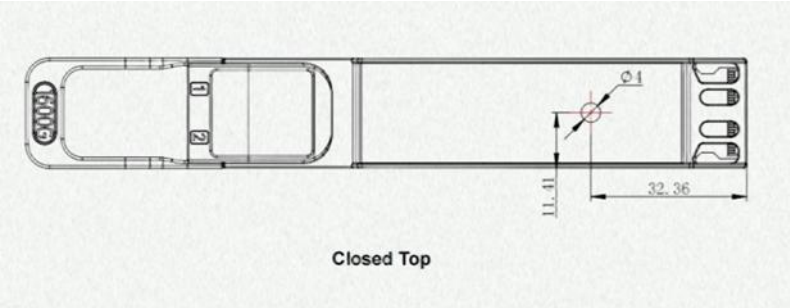

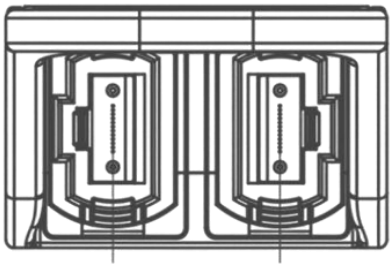

The optical interface port is a dual MPO-12 connector

4. AbsoluteMaximum Ratings

Exceeding the absolute maximum ratings table may cause permanent damage to the device. This is just an emphasized rating, and does not involve the functional operation of the device that exceeds the specifications of this technical specification under these or other conditions. Long-term operation under absolute maximum ratings will affect the reliability of the device.

Parameter	Symbol	Min.	Typical	Max.	Unit
Storage temperature	Ts	-40		+85	℃
3.3V power supply voltage	Vcc	-0.3	3.3	3.6	V
Data input voltage – single ended		-0.3		Vcc+0.3	V
Data input voltage – differential				0.8	V
Relative humidity	RH	5		85	%

1. Exceeding any one of these values may damage the device permanently.
2. This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry. The damage threshold of the module input shall be at least 1600 mV peak to peak differential.

5. Recommended Operations Conditions

For operations beyond the recommended operating conditions, optical and electrical characteristics are not defined, reliability is not implied, and such operations for a long time may damage the module.

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Parameter	Symbol	Min.	Typical	Max.	Unit
Operating case temperature	Tc	0		70	°C
Power supply voltage	Vcc	3.135	3.3	3.465	V
Power dissipation	PD			16	W
Supply Current	Icc			5.1	A
Electrical signal rate per channel (PAM encoded)			53.125		GBd
Optical signal rate per channel (PAM encoded)			53.125		GBd
Power supply noise				66	mVpp
Pre-FEC Bit Error Ratio				2.4x10-4	
Post-FEC Bit Error Ratio				1x10-12	
Receiver differential data output load			100		Ohm
Fiber length (9um SMF)		2		500	m

1. Power Supply specifications, Instantaneous, sustained and steady state current compliant with OSFP MSA Power Classification.
2. 800GAUI-8 operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.
3. 800G DR8 operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.
4. 9μm SMF. The maximum link distance is based on an allocation of 1dB of attenuation and 3 dB total connection and splice loss. The loss of a single connection shall not exceed 0.5dB.

6. General Electrical Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Symbol	Min.	Typical	Max.	Unit
Transceiver power consumption				16	W
Transceiver power supply current, total				5100	mA

1. For control and status signals timing including SCL, SDA, LPWn/PRSn, INT/RSTn, please refer to Control Interface Section.

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7. Reference points

For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a single-mode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 162.9.3 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI . Unless specified otherwise, all receiver measurements and tests defined in 162.9.4 are made at TP3

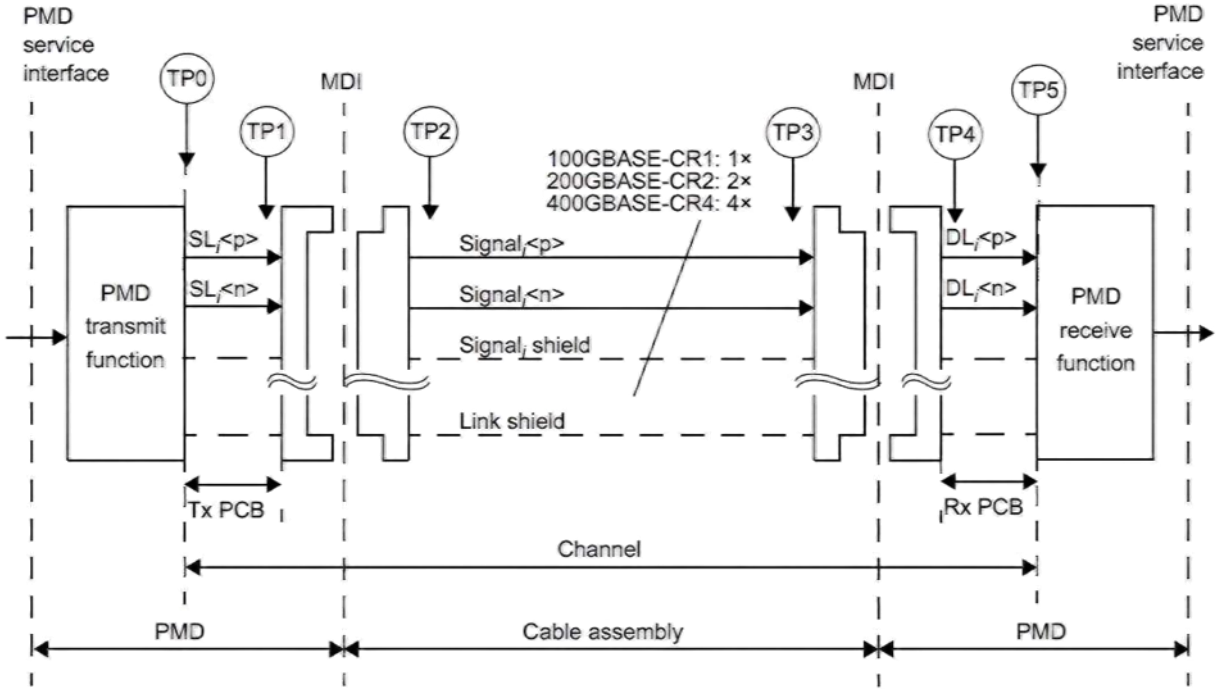

Figure 3: IEEE 802.3ck 100GBASE-CR1, 200GBASE-CR2 or 400GBASE-CR4 link

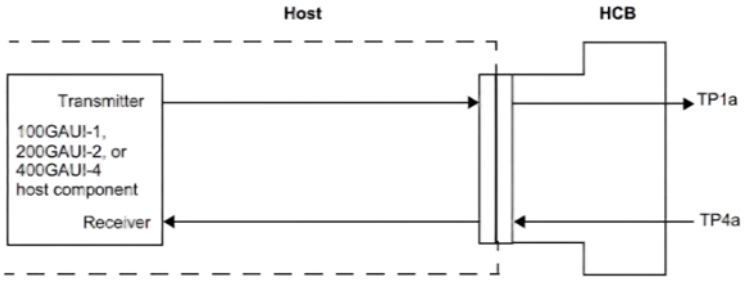

Figure 4: IEEE 802.3ck400GAUI-4compliance points TP1a, TP4a

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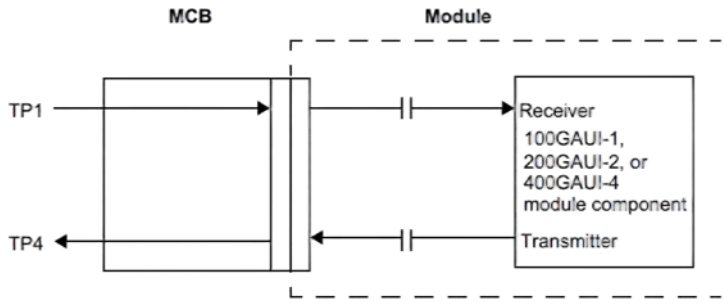

Figure 5: IEEE 802.3dj module compliance points TP1, TP4

8. High Speed Electrical Input Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling rate, per lane (PAM4 encoded)	TP1a		53.125±100 ppm		GBd
Differential peak-peak input voltage tolerance	TP1a	900			mV
DC common-mode voltage	TP1a	-350		2850	mV
Differential termination mismatch	TP1a			10	%
Effective return loss, ERL	TP1a	TBD	802.3ck		dB
Common-mode to common-mode return loss, RLcc	TP1a	Equation (179–9)			dB
Common-mode to differential-mode return loss, RLdc	TP1a	Equation (179–10)			dB
Single-ended voltage tolerance range	TP1a	-0.4		3.3	V

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9. High Speed Electrical Output Characteristics:

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted

Parameter	Test Point	Min.	Typical	Max.	Unit
Signaling rate, per lane (range)	TP4		53.125±100 ppm		GBd
Differential Output Voltage (Long mode)	TP4			845	mV
Differential Output Voltage (Short mode)	TP4			600	mV
DC Common-mode Voltage Tolerance	TP4	-350		2850	mV
Eye Height	TP4	15			mV
Vertical Eye Closure	TP4			12	mV
Effective return loss, ERL	TP4	TBD	802.3ck		dB
Differential Termination Mismatch	TP4			10	%

10. High Speed Optical Transmitter Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Optical Characteristics @TP2 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling speed per lane			53.125±100ppm		GBd
Modulation format			PAM4		
Lane center wavelength	λC	1304.5	1311	1317.5	nm
Side-mode suppression ratio	SMSR	30			dB
Average launch power, each lane	TxAVG	-2.9		4	dBm
Outer optical modulation amplitude (OMAouter),		-0.8			
Each lane for TDECQ<1.4dB	OMAmax	-2.2+TDECQ		4.2	dBm
for 1.4dB≤TDECQ≤3.4dB					
Transmitter and dispersion eye closure for PAM4					
(TDECQ),each lane	TDECQ			3.4	dB
Transmitter eye closure for PAM4 (TECQ) , each lane	TECQ			3.4	dB
|TDECQ-TECQ|				2.5	dB
Transmitter overshoot and undershoot				22	%

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Average Launch power of OFF transmitter,each lane					
Extinction ratio	ER	3.5			dB
Transmitter transition time				17	PS
RIN17.1 OMA				-136	dB/Hz
Optical return loss tolerance				21.4	dB
Transmitter reflectance				-26	dB

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Transmitter reflectance is defined looking into the transmitter.

11. High Speed Optical Transmitter Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Optical Characteristics @TP3 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling speed per lane			53.125±100ppm		GBd
Modulation format			PAM4		
Lane center wavelength	λ_C	1304.5	1311	1317.5	nm
Damage threshold each lane		5			
Average receive power each lane	Rx_{AVG}	-5.9		4	dBm
Receive Power (OMA_{outer}) each lane	Rx_{OMA}			4.2	dBm
Receiver sensitivity (OMA_{outer}),	Sen_{OMA}			-4.2	dBm
stressed receiver sensitivity (OMAouter), each lane				-1.9	dBm
OMAouter of each aggressor lane			4.2		dBm
LOS Assert	LOSA	-15			dBm
LOS De-Assert	LOSD			-10	dBm
LOS hysteresis		0.5			dB

1.Measured with conformance test signal at TP3 for the BER specified in IEEE 802.3bs

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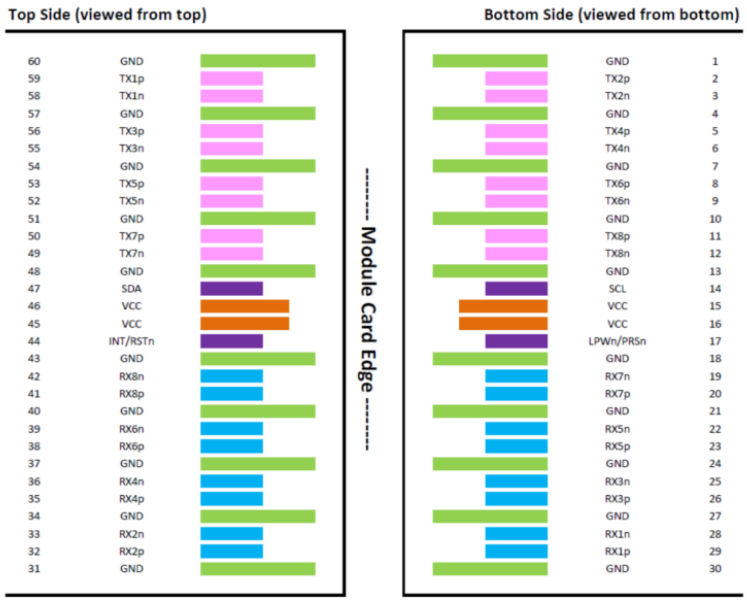
12. Electrical to Optical Channel Mapping

Electrical Channels	Optical Wavelength (nm)
1-8	1311

13. Applications Note:

Pin Definitions



Pin Function Definitions

Pin	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1	1
2	CML-I	Tx2p	Transmitter Data Non-Inverted	3	
3	CML-I	Tx2n	Transmitter Data Inverted	3	
4		GND	Ground	1	1
5	CML-I	Tx4p	Transmitter Data Non-Inverted	3	
6	CML-I	Tx4n	Transmitter Data Inverted	3	

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7		GND	Ground	1	1
8	CML-I	Tx6p	Unused	3	
9	CML-I	Tx6n	Unused	3	
10		GND	Ground	1	1
11	CML-I	Tx8p	Unused	3	
12	CML-I	Tx8n	Unused	3	
13		GND	Ground	1	1
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	3	2
15		VCC	+3.3V Power	2	
16		VCC	+3.3V Power	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode/Module Present	3	
18		GND	Ground	1	1
19	CML-O	Rx7n	Unused	3	
20	CML-O	Rx7p	Unused	3	
21		GND	Ground	1	1
22	CML-O	Rx5n	Unused	3	
23	CML-O	Rx5p	Unused	3	
24		GND	Ground	1	1
25	CML-O	Rx3n	Receiver Data Inverted	3	
26	CML-O	Rx3p	Receiver Data Non-Inverted	3	
27		GND	Ground	1	1
28	CML-O	Rx1n	Receiver Data Inverted	3	
29	CML-O	Rx1p	Receiver Data Non-Inverted	3	
30		GND	Ground	1	1
31		GND	Ground	1	1
32	CML-O	Rx2p	Receiver Data Non-Inverted	3	
33	CML-O	Rx2n	Receiver Data Inverted	3	
34		GND	Ground	1	1
35	CML-O	Rx4p	Receiver Data Non-Inverted	3	
36	CML-O	Rx4n	Receiver Data Inverted	3	
37		GND	Ground	1	1

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38	CML-O	Rx6p	Unused	3	
39	CML-O	Rx6n	Unused	3	
40		GND	Ground	1	1
41	CML-O	Rx8p	Unused	3	
42	CML-O	Rx8n	Unused	3	
43		GND	Ground	1	1
44	Multi-Level	INT/RSTn	Module input/Module Reset	3	
45		VCC	+3.3V Power	2	
46		VCC	+3.3V Power	2	
47	LVCMOS-I/O	SCL	2-wire Serial interface Data	3	2
48		GND	Ground	1	1
49	CML-I	Tx7n	Unused	3	
50	CML-I	Tx7p	Unused	3	
51		GND	Ground	1	1
52	CML-I	Tx5n	Unused	3	
53	CML-I	Tx5p	Unused	3	
54		GND	Ground	1	1
55	CML-I	Tx3n	Transmitter Data Inverted	3	
56	CML-I	Tx3p	Transmitter Data Non-Inverted	3	
57		GND	Ground	1	1
58	CML-I	Tx1n	Transmitter Data Inverted	3	
59	CML-I	Tx1p	Transmitter Data Non-Inverted	3	
60		GND	Ground	1	1

1: OSFP uses common ground (GND) for all signals and supply (power). All are common within the OSFP module and all module voltages are referenced to this potential unless otherwise noted.

2: Open-Drain with pull up resistor on Host.

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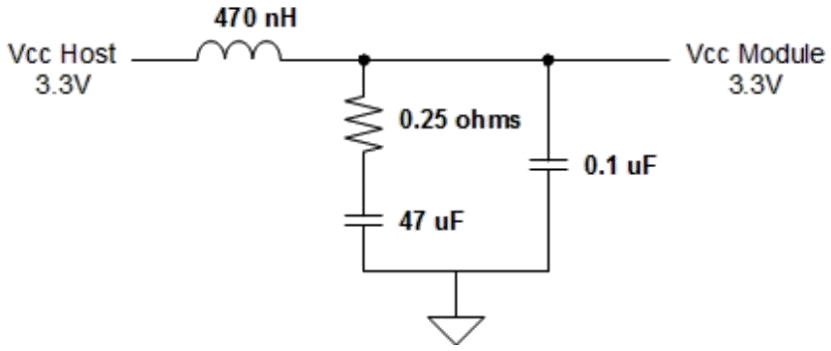

Figure 7: Recommended Host Board Power Supply Filter

For safety and protection of the host system, the power to each OSFP module may be protected by an electronic circuit breaker on the host board which is enabled with the H_PRSn signal such that power is only enabled when the module is fully engaged into the OSFP connector.

Control Interface & Memory Map

The control interface combines dedicated signal lines for LPWn/PRSn, INT/RSTn with two-wire serial (TWS), interface clock (SCL) and data (SDA), signals to provide users rich functionality over an efficient and easily used interface.

SCL and SDA

SCL and SDA are a 2-wire serial interface between the host and module using the I2C protocols. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3Von the host. The pull-up resistor value shall be 1k ohms to 4.7k ohms depending on capacitive load.

This 2-wire interface supports bus speeds:

- Required – I2C Fast-mode (Fm) ≤ 400 kbit/s
- Optional – I2C Fast-mode Plus (Fm+) ≤ 1 Mbit/s

The host shall default to using 100 kbit/s standard-mode I2C when first accessing an unidentified module for backward compatibility. Once the module has been brought out of reset, the host can read the module' s 2-

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wire interface speed register to determine the maximum supported speed the module allows. For an OSFP, the host may then use I2C Fast-mode, I2C Fast-mode Plus Single Data Rate, as indicated by the module. It is optional for the host to change the speed of the 2-wire interface but remaining at a low speed could lead to slow management transactions for modules that require frequent accesses.

SCL and SDA signals follow the electrical specifications of Fast-mode, and Fast-mode Plus as defined in the I2C –bus specification.

SCL and SDA Pin Electrical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit
SCL and SDA	VOL	0		0.4	V
	VOH	VCC-0.5		VCC+0.3	V
SCL and SDA	VIL	-0.3		VCC*0.3	V
	VIH	VCC*0.7		VCC+0.5	V

INT/RSTn

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. The circuit shown in OSFP MSA enables multi-level signaling to provide direct signal control in both directions. Reset is an active low signal on the host which is translated to an active- low signal on the module. Interrupt is an active-high signal on the module which gets translated to an active-low signal on the host.

The INT/RSTn signal operates in 3 voltage zones to indicate the state of Reset for the module and Interrupt for the host. Figure 11 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_INTn signal and the module uses a voltage reference at 1.25V to determine the state of the M_RSTn signal.

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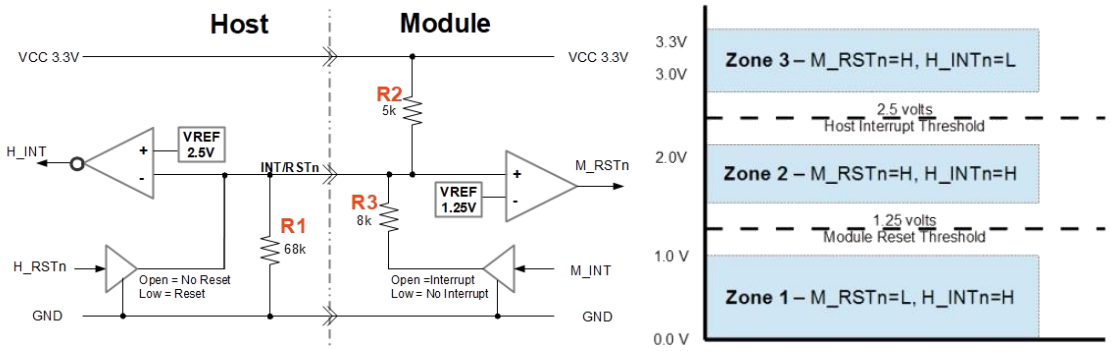

Figure 11: INT/RSTn Voltage Zones

LPWn/PRSn

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present. The circuit shown in OSFP MSA enables multi-level signaling to provide direct signal control in both directions. Low Power mode is an active-low signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host.

The LPWn/PRSn signal operates in 3 voltage zones to indicate the state of Low Power mode for the module and Module Present for the host. Figure 12 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_PRSn signal and the module uses a voltage reference at 1.25V to determine the state of the M_LPWn signal.

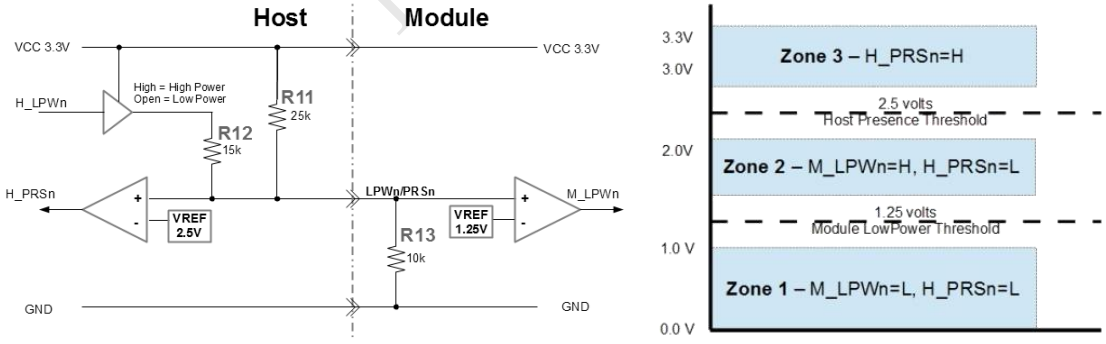

Figure 12: LPWn/PRSn Voltage Zones

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Timing for control and status functions

Parameter	Symbol	Min.	Typical	Max.	Unit
MgmtInit duration	t_init			2000	ms
ResetL assert time	t_reset_init	10			μs
Reset assert time	t_reset			8	s
LPMode assert time	ton_LPMode			200	μs
LPMode de-assert time	toff_LPMode			8	s
IntL assert time	ton_IntL			200	ms
IntL de-assert time	toff_IntL			500	μs
Rx LOS assert time	ton_LOS			100	ms
Tx fault assert time	ton_flag			200	ms
Flag assert time	ton_flag			200	ms
Mask assert time	ton_mask			100	ms
Mask de-assert time	toff_mask			100	ms
Application or rate select change time	t_ratesel			8	s
Rx squelch assert time	ton_Rxsq			15	ms
Rx squelch de-assert time	toff_Rxsq			5000	ms
Tx squelch assert time	ton_Txsq			400	ms
Tx squelch de-assert time	toff_Txsq			5000	ms
Tx disable assert time	ton_txdis			100	ms
Tx disable de-asssert time	toff_txdis			400	ms
Rx output disable assert time	ton_rxdis			100	ms
Rx output disable de-assert time	toff_rxdis			100	ms
Squelch disable assert time	ton_sqdis			100	ms
Squelch disable de-assert time	toff_sqdis			100	ms

Memory Map

The control interface and memory map of the OSFP module is compliant with the CMIS. The OSFP module support I2C interface protocol defined by the CMIS. Access clock frequency is support a minimum of 100 kHz with no clock stretching.

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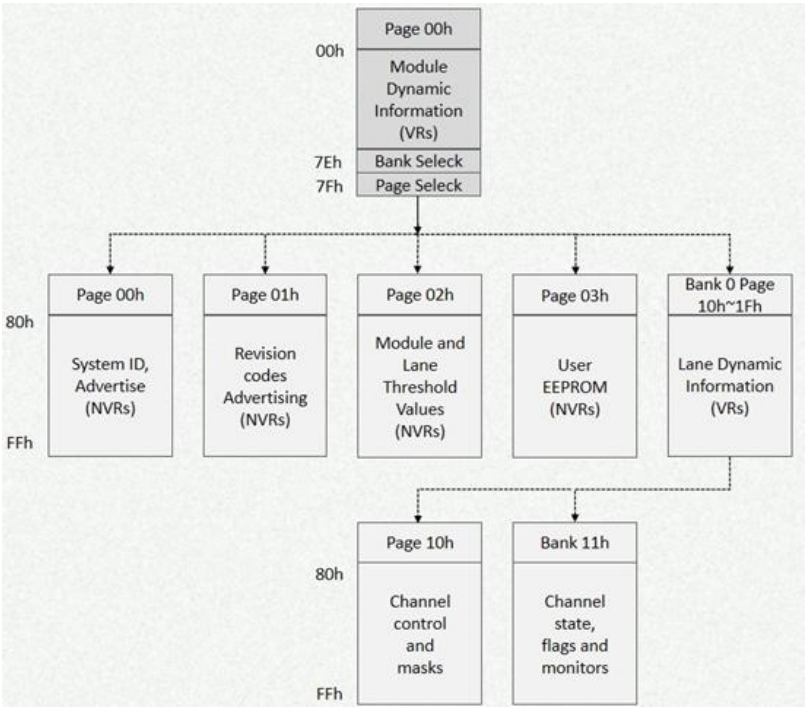
	REVISION：01	AUTHORIZED BY：Andy Yang
	DATE：2026.06.30	CLASSIFICATION：Optical Transceivers



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14. Modification History

Rev.	Comments	Date	Originator	Approval
01	Initial	2026.06.30	Andy Yang	Mike Sun